UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,812	10/30/2003	Bor-Sung Liang	LIAN3019/EM	6893

23364 7590 02/23/2006

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314

EXAMINER	
CODY, DILLON J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,812	LIANG, BOR-SUNG	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 Jan 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, filed 30 October 2003 and information disclosure statement, filed 5 January 2005.

Priority

3. Examiner acknowledges applicant's claim to foreign priority date 15 April 2003.

Information Disclosure Statement

4. Non-patent Literature entry titled "TriCore" has not been considered. Page numbers printed on submitted material do not match page numbers cited on PTO-1449.

Title

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

6. The disclosure is objected to because of the following informalities: The specification contains numerous errors in regards to grammar and readability. Applicant

is advised to repair grammatical mistakes in order to increase enforceability of any future resulting patent.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3 and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (U.S. Patent No. 5,996,070) hereinafter referred to as Yamada.

9. As per claim 1, Yamada discloses

a processor capable of executing conditional instructions, which executes an instruction set including M-bit instructions and N-bit instructions (where M, N are positive integers, M>N), (Fig. 17) *The examiner asserts that the operations 106 and 107 constitute N-bit instructions and the whole packet 250 constitutes an M-bit instruction.*

the instruction set having condition execution instructions and M-bit parallel condition execution instructions, the parallel condition execution instruction having a first N-bit instruction and a second N-bit instruction, the processor comprising: (Col. 16 lines 27-33)

a flag having a state; *The register pointed to by the CC code 105 (Fig. 17) constitutes the flag.*

an instruction fetching device, to fetch at least one instruction to be performed; (Fig. 4 instruction decode unit 2a)

an instruction decoder, to decode the instruction fetched by the instruction fetching device; (Fig. 4 decoders 8 and 9)

an instruction executing device, to execute the instruction outputted by the instruction decoder (Fig. 4 execution units 3 and 4), wherein the state of the flag is set according to a result of executing a condition execution instruction, which indicates a state of condition acceptance or rejection; (Col. 13 line 20-23)

and a mode switching device (Fig. 18 decode unit 2c), to switch the instruction decoder to decode one of the first and the second N-bit instructions according to the state of the flag, so as to be subsequently performed by the instruction executing device, when a parallel condition execution instruction is fetched by the instruction fetching device. (Col. 16 line 34 – col. 17 line 7)

10. As per claim 2, Yamada discloses the processor as claimed in claim 1, wherein, when the instruction executing device executes a condition execution instruction, the

flag is set to a first logic state if the execution results in a condition acceptance, and set to a second logic state if the execution results in a condition rejection. (Col. 13 line 20-23)

11. As per claim 3, Yamada discloses the processor as claimed in claim 2, wherein the first logic state is "true" and the second logic state is "false". (Col. 2 lines 22-24)

12. As per claim 5, Yamada discloses the processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the first logic, the mode switching device switches the instruction decoder to decode the first N-bit instruction, so as to be subsequently performed by the instruction executing device. (Col. 16 line 34 – col. 17 line 7) *Examiner asserts that "first logic state" means that the register(s) pointed to by the condition codes indicate the instruction should progress to execution.*

13. As per claim 6, Yamada discloses the processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the second logic, the mode switching device switches the instruction decoder to decode the second N-bit instruction, so as to be subsequently performed by the instruction executing device. (Col. 16 line 34 – col. 17 line 7) *Examiner asserts that "second logic state" means that the register(s) pointed to by the condition codes indicate the instruction should progress to execution. Further, when s-bit 251 (Fig. 17) equals 0,*

both the first and second instructions proceed to execution.

14. Claims 1-3, 5-6 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (U.S. Patent No. 6,865,662).

15. As per claim 1, Wang discloses

a processor capable of executing conditional instructions, which executes an instruction set including M-bit instructions and N-bit instructions (where M, N are positive integers, M>N), (Fig. 4) *The examiner asserts that the operations 82, 84, 86, 88 constitute N-bit instructions and the whole packet 79 constitutes an M-bit instruction.*

the instruction set having condition execution instructions and M-bit parallel condition execution instructions, the parallel condition execution instruction having a first N-bit instruction and a second N-bit instruction, the processor comprising: (Col. 5 lines 14-25)

a flag having a state; (Fig. 4 condition flag 76)

an instruction fetching device, to fetch at least one instruction to be performed; *The examiner asserts that the instruction must inherently be fetched in order to be executed.*

an instruction decoder, to decode the instruction fetched by the instruction fetching device; *The examiner asserts that the instruction must inherently be decoded in order to be executed.*

an instruction executing device, to execute the instruction outputted by the instruction decoder (Fig. 4 execution units 83, 85, 87 and 89), wherein the state of the flag is set according to a result of executing a condition execution instruction, which indicates a state of condition acceptance or rejection; (Col. 4 line 25-31)

and a mode switching device (Fig. 4 logic elements 75, 92, 94, 96 and 98), to switch the instruction decoder to decode one of the first and the second N-bit instructions according to the state of the flag, so as to be subsequently performed by the instruction executing device, when a parallel condition execution instruction is fetched by the instruction fetching device. (Col. 5 lines 26-45)

16. As per claim 2, Wang discloses the processor as claimed in claim 1, wherein, when the instruction executing device executes a condition execution instruction, the flag is set to a first logic state if the execution results in a condition acceptance, and set to a second logic state if the execution results in a condition rejection. (Col. 4 line 25-31)

17. As per claim 3, Wang discloses the processor as claimed in claim 2, wherein the first logic state is "true" and the second logic state is "false". (Col. 4 line 25-31)

18. As per claim 5, Wang discloses the processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the first logic, the mode switching device switches the instruction decoder to decode the first

N-bit instruction, so as to be subsequently performed by the instruction executing device. (Col. 5 lines 26-45)

19. As per claim 6, Wang discloses the processor as claimed in claim 2, wherein, when the instruction is a parallel condition execution instruction and the flag is on the second logic, the mode switching device switches the instruction decoder to decode the second N-bit instruction, so as to be subsequently performed by the instruction executing device. (Col. 5 lines 26-45)

20. As per claim 10, Wang discloses a method capable of executing conditional instructions in a processor, the processor executing an instruction set with M-bit instructions and N-bit instructions (where M, N are positive integers, M>N), (Fig. 4) *The examiner asserts that the operations 82, 84, 86, 88 constitute N-bit instructions and the whole packet 79 constitutes an M-bit instruction.*

the instruction set having condition execution instructions and M-bit parallel condition execution instructions, the parallel condition execution instruction having a first and a second N-bit instructions, (Col. 5 lines 14-25)

the method comprising:

(A) fetching at least one instruction to be decoded and executed; *The examiner asserts that the instruction in fig. 4 has been fetched. Wang's system must inherently fetch and decode all instructions prior to execution.*

(B) when a condition execution instruction is performed, setting a flag to a first logic state if the execution results in a condition acceptance, and setting the flag to a second logic state if the execution results in a condition rejection; and (Col. 4 line 25-31)

(C) when the instruction fetched is a parallel condition execution instruction, decoding and executing the first N-bit instruction if the flag is on the first logic state, and decoding and executing the second N-bit instruction if the flag is on the second logic state. (Col. 5 lines 26-45)

21. As per claim 11, Wang has taught a method performing the same function as the processor of claim 3, consequently claim 11 is rejected for the same reasons set forth in the rejection of claim 3 above.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada.

24. As per claim 4, Yamada discloses the processor as claimed in claim 2, but fails to disclose wherein the first logic state is "false" and the second logic state is "true".

25. Official notice is taken that it is extremely well known in the art to use a logic 0 to indicate true and a logic 1 to indicate false. The choice of this implementation or the more common 1 = true, 0 = false is largely one of implementation. In some systems, depending on the logical function to be performed, many functions can be implemented with fewer logic gates by using the inverted (0=true, 1=false) logic (inverted logic is also sometimes referred to as "active low" logic). Using fewer logic gates results in smaller implementation, requiring less power and chip size.

26. It would have been obvious to one of ordinary skill in the art at the time of invention to have used inverted logic for the benefit of using fewer gates to implement a circuit, resulting in smaller chip size and lower power consumption.

27. As per claim 7, Yamada discloses the processor as claimed in claim 2, but fails to disclose wherein the condition execution instruction is an M-bit instruction.

28. Official notice is taken that allowing a long-format instruction to set a condition flag is extremely well known in the art. Any instruction, regardless of length, that sets a condition flag reduces processing time for a subsequent instruction, which is dependent on said flag.

29. It would have been obvious to one of ordinary skill in the art at the time of invention to have allowed long-format instructions to set and clear condition flags for the benefit of reduced processing time.

30. As per claim 8, Yamada discloses the processor as claimed in claim 2, but fails to disclose wherein the condition execution instruction is an N-bit instruction.

31. Official notice is taken that allowing a short-format instruction to set a condition flag is extremely well known in the art. Any instruction, regardless of length, that sets a condition flag reduces processing time for a subsequent instruction, which is dependent on said flag.

32. It would have been obvious to one of ordinary skill in the art at the time of invention to have allowed short-format instructions to set and clear condition flags for the benefit of reduced processing time.

33. As per claim 9, Yamada discloses the processor as claimed in claim 1, but fails to disclose wherein M is 32 and N is 16.

34. Official notice is taken that 32-bit and 16-bit instructions are extremely well known in the art. Using such instructions allows the use of smaller components in the processor in comparison to a system with longer instruction formats. Using smaller components means using smaller data and instruction buses, ALUs, register files, etc. resulting in a smaller processor size, requiring less power.

35. It would have been obvious to one of ordinary skill in the art at the time of invention to have included 16-bit and 32-bit instructions in Yamada's processor for the benefit of reduced processor size and power consumption.

36. Further, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been obvious improvements.

37. Claims 4, 7-9 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang.

38. As per claim 4, Wang discloses the processor as claimed in claim 2, but fails to disclose wherein the first logic state is "false" and the second logic state is "true".

39. Official notice is taken that it is extremely well known in the art to use a logic 0 to indicate true and a logic 1 to indicate false. The choice of this implementation or the more common 1 = true, 0 = false is largely one of implementation. In some systems, depending on the logical function to be performed, many functions can be implemented with fewer logic gates by using the inverted (0=true, 1=false) logic (inverted logic is also sometimes referred to as "active low" logic). . Using fewer logic gates results in smaller implementation, requiring less power and chip size.

40. It would have been obvious to one of ordinary skill in the art at the time of invention to have used inverted logic for the benefit of using fewer gates to implement a circuit, resulting in smaller chip size and lower power consumption.

41. As per claim 7, Wang discloses the processor as claimed in claim 2, but fails to disclose wherein the condition execution instruction is an M-bit instruction.

42. Official notice is taken that allowing a long-format instruction to set a condition flag is extremely well known in the art. Any instruction, regardless of length, that sets a condition flag reduces processing time for a subsequent instruction, which is dependent on said flag.

43. It would have been obvious to one of ordinary skill in the art at the time of invention to have allowed long-format instructions to set and clear condition flags for the benefit of reduced processing time.

44. As per claim 8, Wang discloses the processor as claimed in claim 2, but fails to disclose wherein the condition execution instruction is an N-bit instruction.

45. Official notice is taken that allowing a short-format instruction to set a condition flag is extremely well known in the art. Any instruction, regardless of length, that sets a condition flag reduces processing time for a subsequent instruction, which is dependent on said flag.

46. It would have been obvious to one of ordinary skill in the art at the time of invention to have allowed short-format instructions to set and clear condition flags for the benefit of reduced processing time.

47. As per claim 9, Wang discloses the processor as claimed in claim 1, but fails to disclose wherein M is 32 and N is 16.

48. Official notice is taken that 32-bit and 16-bit instructions are extremely well known in the art. Using such instructions allows the use of smaller components in the

processor in comparison to a system with longer instruction formats. Using smaller components means using smaller data and instruction buses, ALUs, register files, etc. resulting in a smaller processor size, requiring less power.

49. It would have been obvious to one of ordinary skill in the art at the time of invention to have included 16-bit and 32-bit instructions in Yamada's processor for the benefit of reduced processor size and power consumption.

50. Further, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are generally not given patentable weight or would have been obvious improvements.

51. As per claim 12, Wang has taught a method performing the same function as the processor of claim 4, consequently claim 12 is rejected for the same reasons set forth in the rejection of claim 4 above.

52. As per claim 13, Wang has taught a method performing the same function as the processor of claim 7, consequently claim 13 is rejected for the same reasons set forth in the rejection of claim 7 above.

53. As per claim 14, Wang has taught a method performing the same function as the processor of claim 8, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 8 above.

54. As per claim 15, Wang has taught a method performing the same function as the processor of claim 9, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 9 above.

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsuo (U.S. Patent No. 6,484,253) teaches a system using conditional execution of two parallel instructions.

Wilson (U.S. Patent No. 6,918,031) teaches a system employing parallel execution and setting condition codes based on execution.

56. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100